REMARKS/ARGUMENTS

Claims 1-15, 44, and 46-54 are pending. Claims 16-43 and 45 have been cancelled. Claims 44 and 46-47 have been amended to address the claim objections and rejections in the examiner's office action. The amended claims are fully supported by the specification. No new matter has been added.

Claims 44, 48-49, and 51 were rejected under section 102(b) as being anticipated by U.S. patent 4,796,211 (Yokouchi). Claims 1-2, 4-5, and 7-14 were rejected under section 103(a) as being unpatentable over U.S. patent 5,479,618 (Steeg) in view of Yokouchi. Claim 3 was rejected under section 103(a) as being unpatentable over Steeg and Yokouchi and U.S. patent 6,505,341 (Harris). Claim 6 and 15 were rejected under section 103(a) as being unpatentable over Steeg and Yokouchi and U.S. patent 5,721,828 (Frisch). Claims 45-47, 50, and 53 were rejected under section 103(a) as being unpatentable over Yokouchi and Steeg. Claim 52 was rejected under section 103(a) as being unpatentable over Yokouchi and U.S. patent 6,298,360 (Muller). Claim 54 was rejected under section 103(a) as being unpatentable over Yokouchi and U.S. patent 6,754,830 (Laiho).

Reconsideration and allowance of the claims are respectfully requested for the reasons discussed in this response. The claims are allowable because each and every limitation is not shown or suggested by the prior art.

CLAIM 1

For example, claim 1 recites "a method of operating a programmable logic integrated circuit." Steeg and Yokouchi, considered individually or in combination, do not teach or suggest a programmable logic integrated circuit. In fact, Steeg teaches quite the opposite. At column 1, lines 54-55, among others, Steeg describes a I/O module with integrated circuitry, which refers to an electronic circuit board with integrated circuits. Moreover, in the paragraph starting at column 3, line 54, Steeg describes two programmable logic circuits 29 and 37 may be integrated circuits such as provided in a Xilinx Inc. data book. There are two integrated circuits, not a programmable logic integrated circuit as in the claim. At the paragraph starting at column

4, line 45, Steeg describes the microelectronic processor 24 as being the model 68HC001 integrated circuit from Motorola Semiconductor. Clearly, Steeg does not teach or suggest a method of operating a programmable logic integrated circuit as recited in claim 1. Nowhere does Yokouchi discuss a programmable logic integrated circuit. Therefore, for at least this reason, claim 1 should be allowable.

Claim 1 further recites "upon receiving the triggered signal output in a reset logic block of the programmable logic integrated circuit, causing reloading of configuration data from an external source into the programmable logic integrated circuit." Steeg and Yokouchi, individually or in combination, do not show or suggest this feature. In the invention, a watchdog timer circuit of the programmable logic integrated circuit is used to detect hardware or software failures (such as an endless loop state), and then upon a failure, to reload the configuration data into the programmable logic integrated circuit. The configuration data is used to reconfigure the programmable logic (e.g., logic array blocks and logic elements) of the integrated circuit. This technique ensures proper operation of the programmable logic integrated circuit and is not taught or suggested by the prior art.

In Steeg, at column 8, lines 49-56, fault logic circuit 76 in first programmable logic circuit 39 generates a RESET/CLEAR signal that is transmitted to second programmable logic circuit 37. Programmable logic circuit 76 is a different programmable logic circuit than programmable logic circuit 39. Figures 4 and 5 show some details of the connections between the two integrated circuits.

The present invention is completely different from Steeg. For the invention, when receiving a triggered signal output in a reset logic block of the programmable logic integrated circuit, this causes reloading of configuration data into the programmable logic integrated circuit. In other words, the watchdog timer circuit and reset logic block reside on the programmable logic integrated circuit. And upon receiving the triggered signal output, the reloading of this same programmable logic integrated will occur. The technique of the invention does not require two different programmable logic circuits as in the prior art. As can be appreciated, using greater numbers of programmable logic integrated circuit increases cost because additional board space

is used and additional power is consumed. Therefore, the invention provides a technique to ensure proper operation of the programmable logic not taught or suggested by the prior art.

For at least this additional reason, claim 1 should be allowable.

Claims 2-15 are dependent on claim 1 and should be allowable for at least similar reasons as claim 1. Claims 2-15 should further be allowable for the additional limitations they recite.

CLAIM 44

Claim 44 recites "a method of operating a programmable logic integrated circuit" and "receiving the triggered signal in a reset logic block of the programmable logic integrated circuit, which causes a reloading of configuration data from an external source into the integrated circuit." As discussed in more detail above, in the method of the present invention, the watchdog timer circuit and reset logic block reside on the programmable logic integrated circuit. And when receiving a triggered signal output, this causes reloading of configuration data into the programmable logic integrated circuit. The prior art, considered individually or in combination, do not show or suggest these features.

For at least this reason, claim 44 should be allowable.

Claims 46-54 are dependent on claim 44 and should be allowable for at least similar reasons as claim 1. Claims 46-54 should further be allowable for the additional limitations they recite.

CONCLUSION

In view of the foregoing, applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400, extension 5213.

Respectfully submitted,

Melvin D. Chan
Reg. No. 39,626

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
MDC:km
60405290 v1